CLAIMS

What is claimed is:

1. An integrated circuit to interface to memory, the integrated circuit comprising:

a first off chip driver calibration terminal to couple to an external pull-up resistor;

a second off chip driver calibration terminal to couple to an external pull-down resistor;

a first switch coupled between the first off chip driver calibration terminal and a voltage reference node; and

a second switch coupled between the second off chip driver calibration terminal and the voltage reference node.

2. The integrated circuit of claim 1, wherein

the first switch and the second switch are selectively closed to generate an internal voltage reference on the voltage reference node with which an input signal may be compared in order to receive data.

3. The integrated circuit of claim 2, wherein

the first switch is selectively closed and the second switch is selectively opened to generate a pull-up

calibration voltage on the voltage reference node to calibrate an off-chip driver.

4. The integrated circuit of claim 3, wherein

the first switch is selectively opened and the second switch is selectively closed to generate a pull-down calibration voltage on the voltage reference node to further calibrate the off-chip driver.

5. The integrated circuit of claim 1, further comprising:

a plurality of input receivers each having a first input coupled to the voltage reference node and a second input coupled to a respective data terminal of a plurality of data terminals.

6. The integrated circuit of claim 5, wherein

each input receiver includes

a comparator having a first input coupled to the voltage reference node and a second input coupled to the respective data terminal, the data terminal to couple to an off-chip output driver for calibration.

7. The integrated circuit of claim 1, further comprising:

a switch controller having a mode input, a first control output coupled to a control input of the first

switch, and a second control output coupled to a control input of the second switch, the switch controller to control the opening and closing of the first switch and the second switch in response to the mode input.

8. The integrated circuit of claim 7, wherein

the first switch and the second switch are selectively closed to generate an internal voltage reference on the voltage reference node with which an input signal may be compared in order to receive data;

the first switch is selectively closed and the second switch is selectively opened to generate a pull-up calibration voltage on the voltage reference node to calibrate an off-chip driver; and

the first switch is selectively opened and the second switch is selectively closed to generate a pull-down calibration voltage on the voltage reference node to further calibrate the off-chip driver.

9. The integrated circuit of claim 1, wherein

the integrated circuit is a memory controller.

10. The integrated circuit of claim 1, wherein

the integrated circuit is a processor.

11. A method in an integrated circuit for interfacing to a memory, the method comprising:

if in an off-chip driver calibration mode for a pull-up, then

selecting a pull-up calibration terminal to be coupled to a voltage reference node to provide a pull-up calibration voltage thereon, and

calibrating a pull-up of an off chip driver;

if in an off-chip driver calibration mode for a pull-down, then

selecting a pull-down calibration terminal to be coupled to the voltage reference node to provide a pull-down calibration voltage thereon, and

calibrating a pull-down of the off chip driver; and,

if in a normal mode to receive data, then

selecting the pull-up calibration terminal and the pull-down calibration terminal to be coupled to the voltage reference node to provide a reference voltage thereon, and

receiving data from a data terminal.

12. The method of claim 11 further comprising:

prior to selecting, calibrating and receiving,

coupling an external pull-up resistor to the pull-up calibration terminal; and

coupling an external pull-down resistor to the pull-down calibration terminal.

13. The method of claim 11, wherein

the receiving data from the data terminal includes

comparing the reference voltage on the voltage reference node with an incoming signal on the data terminal.

14. The method of claim 13, wherein

the calibrating of the pull-up of the off chip driver includes

comparing the pull-up calibration voltage on the voltage reference node with an incoming signal on the data terminal.

15. The method of claim 14, wherein

the calibrating of the pull-down of the off chip driver includes

comparing the pull-down calibration voltage on the voltage reference node with an incoming signal on the data terminal.

16. A system comprising:

a processor for executing instructions and processing data;

a double data rate memory device to store data from the processor and to read data to the processor;

an external pull-up resistor having a first end coupled to a first power supply terminal;

an external pull-down resistor having a first end coupled to a second power supply terminal; and

a memory controller coupled between the double data rate memory device and the processor, the memory controller including

a pull-up calibration terminal coupled to a second end of the external pull-up resistor,

a pull-down calibration terminal coupled to a second end of the external pull-down resistor,

a voltage reference node,

a first switch having a first switch connection coupled to the pull-up calibration terminal and a second switch connection coupled to the voltage reference node, and

a second switch having a first switch connection coupled to the pull-down calibration terminal and a second switch connection coupled to the voltage reference node.

17. The system of claim 16, wherein

the memory controller is an integrated circuit separate from the processor.

18. The system of claim 16, wherein

the processor is an integrated circuit and includes the memory controller.

19. The system of claim 16, wherein

the memory controller further includes

a switch controller having a mode input, a first control output coupled to a control input of the first switch, and a second control output coupled to a control input of the second switch, the switch controller to control the opening and closing of the first switch and the second switch in response to the mode input.

20. The system of claim 19, wherein

the first switch and the second switch are selectively closed to generate an internal voltage reference on the voltage reference node with which an input signal may be compared in order to receive data;

the first switch is selectively closed and the second switch is selectively opened to generate a pull-up calibration voltage on the voltage reference node to calibrate a driver of the DDR memory device; and

the first switch is selectively opened and the second switch is selectively closed to generate a pull-down calibration voltage on the voltage reference node to further calibrate the driver of the DDR memory device.

21. A processor for a computer system, the processor including:

a memory controller to interface to memory, the memory controller having

a pull-up calibration terminal to couple to an external pull-up resistor,

a pull-down calibration terminal to couple to an external pull-down resistor,

a voltage reference node,

a first switch coupled between the pull-up calibration terminal and the voltage reference node, and

a second switch coupled between the pull-down calibration terminal and the voltage reference node.

22. The processor of claim 21, wherein

the memory controller further has

a switch controller having a mode input, a first control output coupled to a control input of the first switch, and a second control output coupled to a control input of the second switch, the switch controller to control the opening and closing of the first switch and the second switch in response to the mode input.

23. The processor of claim 22, wherein

the first switch and the second switch are selectively closed to generate an internal voltage reference on the voltage reference node with which an input signal may be compared in order to receive data from a driver of a DDR memory device;

the first switch is selectively closed and the second switch is selectively opened to generate a pull-up calibration voltage on the voltage reference node to calibrate the driver of the DDR memory device; and

the first switch is selectively opened and the second switch is selectively closed to generate a pull-down calibration voltage on the voltage reference node to further calibrate the driver of the DDR memory device.

24. A packaged integrated circuit to interface to memory, the packaged integrated circuit comprising:

a first off-chip driver calibration terminal to couple to a first external resistor;

a second off-chip driver calibration terminal to couple to a second external resistor;

a first plurality of field effect transistors having sources coupled in parallel together to the first off-chip driver calibration terminal and drains coupled in parallel together to a voltage reference node; and

a second plurality of field effect transistors having drains coupled in parallel together to the second

off-chip driver calibration terminal and sources coupled in parallel together to the voltage reference node.

25. The packaged integrated circuit of claim 24 wherein the first plurality of field effect transistors and the second plurality of field effect transistors are p-channel field effect transistors.

26. The packaged integrated circuit of claim 24 wherein the first plurality of field effect transistors and the second plurality of field effect transistors are n-channel field effect transistors.

27. The packaged integrated circuit of claim 24 wherein the first plurality of field effect transistors are p-channel field effect transistors, and the second plurality of field effect transistors are n-channel field effect transistors.

28. The packaged integrated circuit of claim 24 wherein the first plurality of field effect transistors are n-channel field effect transistors, and the second plurality of field effect transistors are p-channel field effect transistors.

29. The packaged integrated circuit of claim 24 wherein

the first plurality of field effect transistors are p-channel field effect transistors and n-channel field effect transistors having sources coupled in parallel together and drains coupled in parallel together, and

the second plurality of field effect transistors are p-channel field effect transistors and n-channel field effect transistors having sources coupled in parallel together and drains coupled in parallel together.

30. The packaged integrated circuit of claim 24 further comprising:

a switch controller having a mode input, a first plurality of switch control signals coupled to respective gates of the first plurality of field effect transistors, a second plurality of switch control signals coupled to respective gates of the second plurality of field effect transistors, the switch controller to control the switching of the first and second plurality of field effect transistors.

31. The packaged integrated circuit of claim 24 further comprising:

a plurality of input receivers each having a first input coupled to the voltage reference node and a second input coupled to respective data terminals to receive data.

32. The packaged integrated circuit of claim 31, wherein each input receiver includes

a comparator having a first input coupled to the voltage reference node and a second input coupled to a respective data terminal to calibrate a pull-up and a pull-down of an off-chip output driver.

33. The packaged integrated circuit of claim 32, wherein the comparator of each input receiver further to receive data by comparing a reference voltage on the reference node with an input signal on the respective data terminal.